IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

In Re Application of:	
Mehra, Pankaj	Examiner: Zhu, Bo Hui Alvin
Attorney Docket 200301299-3	Group Art Unit: 2619
Serial No. 10/722,180	Confirmation No: 7005
Filing Date: November 24, 2003	
For: NETWORK AND METHOD OF CONFIGURING A NETWORK	

APPEAL BRIEF

To: Mail Stop Appeal Brief - Patents
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

The Appellant herewith respectfully submits the following appeal brief.

This brief contains items under the following headings as required by 37 CFR §41.37 and MPEP §1206:

1. Real Party In Interest
2. Related Appeals, Interferences and Judicial Proceedings
3. Status of Claims
4. Status of Amendments
5. Summary of Claimed Subject Matter
6. Grounds of Rejection to be Reviewed on Appeal
7. Argument

Appendix A	Claims
Appendix B	Evidence
Appendix C	Related Proceedings

1. REAL PARTY IN INTEREST

The real party in interest in the above-referenced patent application is Hewlett-Packard Development Company, LP, a limited partnership established under the laws of the State of Texas and having a principal place of business at 20555 S.H. 249 Houston, TX 77070, U.S.A. (hereinafter "HPDC"). HPDC is a Texas limited partnership and is a wholly-owned affiliate of Hewlett-Packard Company, a Delaware Corporation, headquartered in Palo Alto, CA. The general or managing partner of HPDC is HPQ Holdings, LLC.

2. RELATED APPEALS AND INTERFERENCES

Appellant and the undersigned attorney are not aware of any other appeals or interferences which will directly affect or be directly affected by or having a bearing on the Board's decision in the pending appeal.

3. STATUS OF CLAIMS

Claims 1-44 are currently pending in the present application. The Appellant is appealing the rejections of claims 1-44. See, Claims Appendix.

Claims 1-7, 11-14, 16-21, 29-37 and 41-43 stand rejected under 35 U.S.C. 102(b) as being anticipated by Baty et al., U.S. Patent 5,243,704. Claims 8-10, 15, 22-28 and 38-40 stand rejected under 35 U.S.C. 103(a) as being unpatentable over Baty in view of Kim, U.S. Patent 5,892,932. Claim 44 stands rejected under 35 U.S.C. 103(a) as being unpatentable over Baty.

4. STATUS OF AMENDMENTS

No amendments were filed or entered subsequent to the Final Office Action of March 11, 2008.

5. SUMMARY OF THE CLAIMED SUBJECT MATTER

The invention as claimed is summarized below with reference numerals and references to the specification and drawings. The invention is broadly set forth in the language corresponding to independent claims 1, 16 and 32 and dependent claims 3-7, 11-12, 18-21, 29-30, 34-37 and 41-42. Discussions about elements of the invention can be found at least in the locations in the specification and drawings cited in the claims below.

1. A multi-fabric (fabric of FIG. 7 including 202, 204, 206, 210 and 212, fabric of FIG. 8 including 214, 216, 220, 222, and 224, combined in FIG. 6) interconnection system [paragraphs 2-4, 38, 39, 44, 51, 55, 56, 86], comprising:

a plurality of first nodes interconnected as a balanced incomplete block design of the form 2-(v, k, 1) = b [paragraph 85], wherein v first nodes (190, 192, 194, 196, 200), arranged in b groups (202, 204, 206, 210, 212, 214, 216, 220, 222, 224) of k (e.g., 190 and 192 in 202) first nodes, are interconnected such that each pair of first nodes appears in only one group of the b groups (e.g., 190 and 192 in 202) [FIGS. 6-14, paragraphs 85-87], and

a plurality of first forwarding nodes (e.g., 312, 322, 392, 402) configured to interconnect the plurality of first nodes [paragraphs 94, 95];

a plurality of sets (230-236, 242-250 and 254-262) of second nodes (230, 232, 234, 236, 242, 244, 246, 250, 254,

256, 260, 262), wherein each second node is connected to one of the first nodes, and wherein each of the second nodes is interconnected to every other second node [FIGS. 9-14, paragraph 90].

3. The interconnection system of claim 1, wherein each first node (e.g., 190) includes at least one first switch (e.g., 240) [paragraphs 90 and 92-98].

4. The interconnection system of claim 3, wherein each second node (e.g., 230) in said plurality of sets of second nodes is interconnected to other second nodes (e.g., 232-236) via said at least one first switch (e.g., 240) [FIGS. 9, 10, 14; paragraphs 90 and 92-98].

5. The interconnection system of claim 4, wherein each of said plurality of sets (e.g., 230-236) of second nodes is interconnected to another (e.g., 242-250) of said plurality of sets of second nodes via said at least one first switch (e.g., 240) [FIGS. 9, 10, 14; paragraphs 90 and 92-98].

6. The interconnection system of claim 4, wherein said at least one first switch (e.g., 240) interconnects one of said plurality of sets of second nodes (e.g., 230-236) to another of said plurality of sets of second nodes (e.g., 242-250) [FIGS. 9, 10, 14; paragraphs 90 and 92-98].

7. The interconnection system of claim 4, wherein said at least one first switch (e.g., 240) is shared with at least two of said plurality of sets of second nodes (e.g., 230-236 and second nodes connected to V2 192) [FIGS. 9, 10, 14; paragraphs 90, 92-98 and 103].

11. The interconnection system of claim 1, wherein each second node (e.g., 230) in said plurality of sets of second nodes is configured with at least two communications ports (e.g., for switches 240 and 332) [FIG. 14; paragraph 95].

12. The interconnection system of claim 1, wherein connections between second nodes in said plurality of sets of second nodes are partitioned into a plurality of incomplete fabrics (Fx and Fy) [FIGS. 12-14; paragraphs 100, 101].

16. A method for configuring a communications network [paragraphs 2-4, 38, 39, 44, 51, 55, 56], comprising:

configuring interconnections of a plurality of first nodes as a balanced incomplete block design of the form 2-(v, k, 1) = b [paragraph 85], wherein v first nodes (190, 192, 194, 196, 200), arranged in b groups (202, 204, 206, 210, 212, 214, 216, 220, 222, 224) of k (e.g., 190 and 192 in 202) first nodes, are interconnected such that a pair of first nodes appears in only one group of the b groups (e.g., 190 and 192 in 202) [FIGS. 6-14, paragraphs 85-87]; and

configuring interconnections of a plurality of sets (230-236, 242-250 and 254-262) of second nodes (230, 232, 234, 236, 242, 244, 246, 250, 254, 256, 260, 262) to the plurality of first nodes, wherein each second node is interconnected to every other second node [FIGS. 9-14, paragraph 90].

18. The method of claim 16, wherein each of said plurality of first nodes (e.g., 190) includes at least one switch (e.g., 240) [paragraphs 90 and 92-98].

19. The method of claim 18, further comprising configuring interconnections of each second node (e.g., 230) in said plurality of sets of second nodes to every other second node

(e.g., 232-236) via said at least one switch (e.g., 240) [FIGS. 9, 10, 14; paragraphs 90 and 92-98].

20. The method of claim 18, wherein said at least one switch (e.g., 240) interconnects one set of second nodes (e.g., 230-236) in said plurality of sets of second nodes to another set of second nodes (e.g., 242-250) in said plurality of sets of second nodes [FIGS. 9, 10, 14; paragraphs 90 and 92-98].

21. The method of claim 18, wherein at least one of said at least one switches (e.g., 240) is shared by at least two sets of second nodes in said plurality of sets of second nodes (e.g., 230-236 and second nodes connected to V2 192) [FIGS. 9, 10, 14; paragraphs 90, 92-98 and 103].

29. The method of claim 16, wherein each second node (e.g., 230) in said plurality of sets of second nodes is configured with at least two communications ports (e.g., for switches 240 and 332) [FIG. 14; paragraph 95].

30. The method of claim 16, further comprising partitioning connections among second nodes in said plurality of sets of second nodes into a plurality of incomplete fabrics (Fx and Fy) [FIGS. 12-14; paragraphs 100, 101].

32. A method for converting a mathematical design to a physical communications network [paragraphs 2-4, 38, 39, 44, 51, 55, 56], comprising:

providing a mathematical representation of a plurality of connected first nodes in the form of a balanced incomplete block design defined as 2-(v, k, 1) = b [paragraph 85], wherein v first nodes (190, 192, 194, 196, 200), arranged in b groups (202, 204, 206, 210, 212, 214, 216, 220, 222, 224) of k

first nodes (e.g., 190 and 192 in 202), are interconnected such that a pair of first nodes appears in only one group of the *b* groups (e.g., 190 and 192 in 202) [FIGS. 6-14, paragraphs 85-87];

converting the mathematical representation to a physical design in which a plurality of first forwarding nodes (e.g., 312, 322, 392, 402) interconnect the plurality of first nodes [paragraphs 94, 95]; and

assigning a plurality of sets (230-236, 242-250 and 254-262) of second nodes (230, 232, 234, 236, 242, 244, 246, 250, 254, 256, 260, 262) to one of the first nodes; such that each of the second nodes is interconnected to every other node.

34. The method of claim 32, wherein each of said plurality of connected first nodes (e.g., 190) includes at least one switch (e.g., 240) [paragraphs 90 and 92-98].

35. The method of claim 34, further comprising configuring interconnections of each second node (e.g., 230) of said plurality of sets of second nodes to other second nodes (e.g., 232-236) via said at least one switch (e.g., 240) [FIGS. 9, 10, 14; paragraphs 90 and 92-98].

36. The method of claim 34, wherein said at least one switch (e.g., 240) interconnects one of said plurality of sets of second nodes (e.g., 230-236) to another of said plurality of sets of second nodes (e.g., 242-250) [FIGS. 9, 10, 14; paragraphs 90 and 92-98].

37. The method of claim 34, wherein at least one of said at least one second switches (e.g., 240) is shared by at least two of said plurality of sets of second nodes (e.g., 230-236 and second nodes connected to V2 192) [FIGS. 9, 10, 14;

paragraphs 90, 92-98 and 103].

41. The method of claim 32, wherein each second node (e.g., 230) in said plurality of sets of second nodes is configured with at least two communications ports (e.g., for switches 240 and 332) [FIG. 14; paragraph 95].

42. The method of claim 32, further comprising partitioning connections among second nodes in said plurality of sets of second nodes into a plurality of incomplete fabrics (Fx and Fy) [FIGS. 12-14; paragraphs 100, 101].

6. GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

Appellant appeals the final rejection of claims 1-7, 11-14, 16-21, 29-37 and 41-43 under 35 U.S.C. 102(b) as being anticipated by Baty et al., U.S. Patent 5,243,704. Appellant also appeals the final rejection of claims 8-10, 15, 22-28 and 38-40 under 35 U.S.C. 103(a) as being unpatentable over Baty in view of Kim, U.S. Patent 5,892,932. Appellant also appeals the final rejection of claim 44 under 35 U.S.C. 103(a) as being unpatentable over Baty.

7. ARGUMENT

I. Rejection of claims 1-7, 11-14, 16-21, 29-37 and 41-43 under 35 U.S.C. 102(b)

CLAIM 1

Claim 1 is reprinted as follows for convenience:

A multi-fabric interconnection system, comprising:

a plurality of first nodes interconnected as a balanced incomplete block design of the form 2-(v, k, 1) = b, wherein v first nodes, arranged in b groups of k first nodes, are interconnected such that each pair of first nodes appears in only one group of the b groups, and

a plurality of first forwarding nodes configured to interconnect the plurality of first nodes;

a plurality of sets of second nodes, wherein each second node is connected to one of the first nodes, and wherein each of the second nodes is interconnected to every other second node.

At least the above highlighted features are not anticipated or suggested by the cited references and would not have been obvious to a person with ordinary skill in the art having the cited references. The Office Action mailed July 26, 2007 indicates that Baty's nodes (e.g., 12) correspond with the claimed first nodes, that Baty's busses (e.g., 26) correspond with the claimed first forwarding nodes, and that Baty's ports (e.g., 12a) correspond with the claimed second nodes. Applicant respectfully disagrees, and believes that this broad an interpretation of the term "node" leaves the term with practically no meaning at all. Applicant has

applied a broad definition to the term "node". For example, paragraph 54 gives a number of examples for end nodes: "In doing so, each end node, such as a computer, network-attached I/O device, or processor, has more than two network interface ports." Clearly, however, the term node is not used by the Applicant to refer to a bus or a port as in the cited portions of Baty. In fact, paragraph 54 of Applicant's specification indicates that according to one disclosed design principle, an end node has more than two network interface ports. It would be nonsensical to interpret Baty's ports (e.g., 12a) as a node of claim 1 when that port might contain more than two ports itself. Furthermore, Baty and Applicant's specification both use and distinguish the terms "node", "port" and "bus" (see Baty col. 3, lines 62-67 and Applicant's paragraph 3), so to interpret Baty's nodes, ports and busses all as nodes ignores the definitions of these terms both in Applicant's specification and in Baty. Speaking generally about the different technology contemplated by Baty and Applicant's invention, Baty is directed at a switchless, direct interconnection network, while Applicant's invention is directed at a design methodology for switched multi-fabric networks of various topologies and providing for redundant paths to route around congestion. (See, e.g., paragraphs 2, 4 and 38.)

The Examiner also takes the position that Baty discloses a balanced incomplete block design of the form 2-(v, k, 1)=b where v=7, k=3 and b=7 (section 1, paragraph 1 on page 2 of final Office Action). This means that Baty would have 7 first nodes arranged in 7 groups with 3 first nodes in each of the 7 groups. Claim 1 further requires that the first nodes are "interconnected such that each pair of first nodes appears in only one group of the b groups". Thus, each pair of the 7 first nodes must appear in only one of the 7 groups. The

Examiner has not identified the groups or the group members, or how each pair of Baty's 7 first nodes would appear in only one of the 7 groups. The Examiner has also failed to identify the multiple fabrics in the claimed multi-fabric system.

Appellant therefore believes that claim 1 is allowable over the cited reference and respectfully requests reversal of the rejection.

CLAIM 2

Solely for the purposes of this appeal, claim 2 stands or falls with claim 1.

CLAIM 3

Claim 3 is reprinted as follows for convenience:

The interconnection system of claim 1, **wherein each first node includes at least one first switch.**

The Examiner takes the position that Baty's processing section 42 comprises a switch on a node. Appellant respectfully disagrees. Baty teaches that the processing sections on the nodes 12-24 are "functional units of a digital data processing system" (col. 4, lines 48-50) including three central processing units, a network interface, two peripheral controllers and a shared random access memory unit (col. 4, lines 50-54). Baty clearly does not disclose that "each first node includes at least one first switch." The Examiner has cited Baty, col. 5, lines 12-31 as disclosing the interconnection of second nodes by a switch on a node. However, this section of Baty interface circuitry on each node that determines which port to send communications from. This

clearly does not disclose the interconnection of second nodes by a switch on a node.

CLAIM 4

Claim 4 is reprinted as follows for convenience:

The interconnection system of claim 3, **wherein each second node in said plurality of sets of second nodes is interconnected to other second nodes via said at least one first switch.**

Again, Baty does not disclose that "each first node includes at least one first switch." Baty teaches that the processing sections on the nodes 12-24 are "functional units of a digital data processing system" (col. 4, lines 48-50) including three central processing units, a network interface, two peripheral controllers and a shared random access memory unit (col. 4, lines 50-54). Baty also does not teach that each second node is interconnected to other second nodes by a switch on a first node. Even if Baty's ports (e.g., 12a) anticipate the claimed second nodes, Baty clearly does not teach that each port is interconnected to other ports by a switch on the first node, particularly with the network connections addressed in Appellant's claims. For example, Baty's random access memory unit is clearly not a switch that performs network interconnections of the three ports on the random access memory unit node. The Examiner has cited Baty, col. 5, lines 12-31 as disclosing the interconnection of second nodes by a switch on a node. However, this section of Baty interface circuitry on each node that determines which port to send communications from. This clearly does not disclose the interconnection of second nodes by a switch on a

node.

CLAIM 5

Claim 5 is reprinted as follows for convenience:

The interconnection system of claim 4, **wherein each of said plurality of sets of second nodes is interconnected to another of said plurality of sets of second nodes via said at least one first switch.**

Again, Baty does not disclose that "each first node includes at least one first switch." Baty teaches that the processing sections on the nodes 12-24 are "functional units of a digital data processing system" (col. 4, lines 48-50) including three central processing units, a network interface, two peripheral controllers and a shared random access memory unit (col. 4, lines 50-54). Baty also does not teach that each second node is interconnected to other second nodes by a switch on a first node. Even if Baty's ports (e.g., 12a) anticipate the claimed second nodes, Baty clearly does not teach that each port is interconnected to other ports by a switch on the first node, particularly with the network connections addressed in Appellant's claims. For example, Baty's random access memory unit is clearly not a switch that performs network interconnections of the three ports on the random access memory unit node. Furthermore, if the three ports on each of Baty's nodes comprise a set as indicated by the Examiner with respect to claim 1, then the processing section (e.g., 42) on one node (e.g., 12) would not act as a switch to connect a port (e.g., 12a) on that node (e.g., 12) with a port (e.g., 14a) on another node (e.g., 14). The Examiner has cited Baty, col. 5, lines 12-31 as disclosing the

interconnection of second nodes by a switch on a node. However, this section of Baty interface circuitry on each node that determines which port to send communications from. This clearly does not disclose the interconnection of second nodes by a switch on a node.

CLAIM 6

Claim 6 is reprinted as follows for convenience:

The interconnection system of claim 4, **wherein said at least one first switch interconnects one of said plurality of sets of second nodes to another of said plurality of sets of second nodes.**

Again, Baty does not disclose that "each first node includes at least one first switch." Baty teaches that the processing sections on the nodes 12-24 are "functional units of a digital data processing system" (col. 4, lines 48-50) including three central processing units, a network interface, two peripheral controllers and a shared random access memory unit (col. 4, lines 50-54). Baty also does not teach that each second node is interconnected to other second nodes by a switch on a first node. Even if Baty's ports (e.g., 12a) anticipate the claimed second nodes, Baty clearly does not teach that each port is interconnected to other ports by a switch on the first node, particularly with the network connections addressed in Appellant's claims. For example, Baty's random access memory unit is clearly not a switch that performs network interconnections of the three ports on the random access memory unit node. Furthermore, if the three ports on each of Baty's nodes comprise a set as indicated by the Examiner with respect to claim 1, then the processing

section (e.g., 42) on one node (e.g., 12) would not act as a switch to connect a port (e.g., 12a) on that node (e.g., 12) with a port (e.g., 14a) on another node (e.g., 14). The Examiner has cited Baty, col. 5, lines 12-31 as disclosing the interconnection of second nodes by a switch on a node. However, this section of Baty interface circuitry on each node that determines which port to send communications from. This clearly does not disclose the interconnection of second nodes by a switch on a node.

CLAIM 7

Claim 7 is reprinted as follows for convenience:

The interconnection system of claim 4, **wherein said at least one first switch is shared with at least two of said plurality of sets of second nodes.**

Again, Baty does not disclose that "each first node includes at least one first switch." Baty teaches that the processing sections on the nodes 12-24 are "functional units of a digital data processing system" (col. 4, lines 48-50) including three central processing units, a network interface, two peripheral controllers and a shared random access memory unit (col. 4, lines 50-54). Furthermore, if the three ports on each of Baty's nodes comprise a set as indicated by the Examiner with respect to claim 1, then the processing section (e.g., 42) on one node (e.g., 12) would not be shared with at least two of the plurality of sets of second nodes. For example, set 12a, 12b and 12c does not share processing section 42 with set 14a, 14b and 14c. The Examiner has stated with respect to claim 7 that "the switch in node 12 is shared with 12a, 12b and 12c". However, the Examiner indicated with

respect to claim 1 that ports 12a, 12b and 12c are supposed to be a single set, not "at least two of said plurality of sets" as in claim 7.

CLAIM 11

Claim 11 is reprinted as follows for convenience:

The interconnection system of claim 1, **wherein each second node in said plurality of sets of second nodes is configured with at least two communications ports.**

Again, Appellant strongly disagrees with the interpretation of claim language applied by the Examiner. The Examiner has indicated that Baty's port 12a is a second node as in Appellant's claim 11, and that the connections from port 12a on trace 46a and bus 26 are communications ports on Baty's port 12a. Baty's ports thus each have two ports. Appellant believes that the Examiner has applied such broad interpretations of terms in both Appellant's claims and Baty's disclosure that the meanings given in both documents become meaningless.

CLAIM 12

Claim 12 is reprinted as follows for convenience:

The interconnection system of claim 1, **wherein connections between second nodes in said plurality of sets of second nodes are partitioned into a plurality of incomplete fabrics.**

The Examiner takes the position that Baty's ports 12a and

12b are connected by interface section 40 and processing section 42, and that this comprises an incomplete fabric. Appellant respectfully disagrees that Baty's interface section 40 and processing section 42 comprise a fabric of any sort that connects ports 12a and 12b. Baty does not disclose or suggest that communications pass between ports 12a and 12b via interface section 40 and processing section 42.

CLAIMS 13-14

Solely for the purposes of this appeal, claims 13-14 stand or fall with claim 1.

CLAIM 16

Claim 16 is reprinted as follows for convenience:

A method for configuring a communications network, comprising:

configuring interconnections of a plurality of first nodes as a balanced incomplete block design of the form 2-(v, k, 1) = b, wherein v first nodes, arranged in b groups of k first nodes, are interconnected such that a pair of first nodes appears in only one group of the b groups; and

configuring interconnections of a plurality of sets of second nodes to the plurality of first nodes, wherein each second node is interconnected to every other second node.

As discussed above with respect to claim 1, the computing system architecture of claim 10 is allowable at least because Baty does not disclose or suggest a plurality of sets of second nodes being interconnected with a plurality of first nodes. Baty's ports (e.g., 12a) are not nodes as defined either in Applicant's specification or by Baty.

Appellant therefore believes that claim 16 is allowable over the cited references and respectfully requests reversal of the rejection.

CLAIM 17

Solely for the purposes of this appeal, claim 17 stands or falls with claim 16.

CLAIM 18

Claim 18 is reprinted as follows for convenience:

The method of claim 16, **wherein each of said plurality of first nodes includes at least one switch.**

The Examiner takes the position that Baty's processing section 42 comprises a switch on a node. Appellant respectfully disagrees. Baty teaches that the processing sections on the nodes 12-24 are "functional units of a digital data processing system" (col. 4, lines 48-50) including three central processing units, a network interface, two peripheral controllers and a shared random access memory unit (col. 4, lines 50-54). Baty clearly does not disclose that "each first node includes at least one first switch." The Examiner has cited Baty, col. 5, lines 12-31 as disclosing the interconnection of second nodes by a switch on a node. However, this section of Baty interface circuitry on each node that determines which port to send communications from. This clearly does not disclose the interconnection of second nodes by a switch on a node.

CLAIM 19

Claim 19 is reprinted as follows for convenience:

The method of claim 18, **further comprising configuring interconnections of each second node in said plurality of sets of second nodes to every other second node via said at least one switch.**

Again, Baty does not disclose that "each first node includes at least one first switch." Baty teaches that the processing sections on the nodes 12-24 are "functional units of a digital data processing system" (col. 4, lines 48-50) including three central processing units, a network interface, two peripheral controllers and a shared random access memory unit (col. 4, lines 50-54). Baty also does not teach that each second node is interconnected to other second nodes by a switch on a first node. Even if Baty's ports (e.g., 12a) anticipate the claimed second nodes, Baty clearly does not teach that each port is interconnected to other ports by a switch on the first node, particularly with the network connections addressed in Appellant's claims. For example, Baty's random access memory unit is clearly not a switch that performs network interconnections of the three ports on the random access memory unit node. The Examiner has cited Baty, col. 5, lines 12-31 as disclosing the interconnection of second nodes by a switch on a node. However, this section of Baty interface circuitry on each node that determines which port to send communications from. This clearly does not disclose the interconnection of second nodes by a switch on a node.

CLAIM 20

Claim 20 is reprinted as follows for convenience:

The method of claim 18, **wherein said at least one switch interconnects one set of second nodes in said plurality of sets of second nodes to another set of second nodes in said plurality of sets of second nodes.**

Again, Baty does not disclose that "each first node includes at least one first switch." Baty teaches that the processing sections on the nodes 12-24 are "functional units of a digital data processing system" (col. 4, lines 48-50) including three central processing units, a network interface, two peripheral controllers and a shared random access memory unit (col. 4, lines 50-54). Baty also does not teach that each second node is interconnected to other second nodes by a switch on a first node. Even if Baty's ports (e.g., 12a) anticipate the claimed second nodes, Baty clearly does not teach that each port is interconnected to other ports by a switch on the first node, particularly with the network connections addressed in Appellant's claims. For example, Baty's random access memory unit is clearly not a switch that performs network interconnections of the three ports on the random access memory unit node. Furthermore, if the three ports on each of Baty's nodes comprise a set as indicated by the Examiner with respect to claim 1, then the processing section (e.g., 42) on one node (e.g., 12) would not act as a switch to connect a port (e.g., 12a) on that node (e.g., 12) with a port (e.g., 14a) on another node (e.g., 14). The Examiner has cited Baty, col. 5, lines 12-31 as disclosing the interconnection of second nodes by a switch on a node. However, this section of Baty interface circuitry on each node that determines which port to send communications from. This

clearly does not disclose the interconnection of second nodes by a switch on a node.

CLAIM 21

Claim 21 is reprinted as follows for convenience:

The method of claim 18, **wherein at least one of said at least one switches is shared by at least two sets of second nodes in said plurality of sets of second nodes.**

Again, Baty does not disclose that "each first node includes at least one first switch." Baty teaches that the processing sections on the nodes 12-24 are "functional units of a digital data processing system" (col. 4, lines 48-50) including three central processing units, a network interface, two peripheral controllers and a shared random access memory unit (col. 4, lines 50-54). Furthermore, if the three ports on each of Baty's nodes comprise a set as indicated by the Examiner with respect to claim 1, then the processing section (e.g., 42) on one node (e.g., 12) would not be shared with at least two of the plurality of sets of second nodes. For example, set 12a, 12b and 12c does not share processing section 42 with set 14a, 14b and 14c. The Examiner has stated with respect to claim 7 that "the switch in node 12 is shared with 12a, 12b and 12c". However, the Examiner indicated with respect to claim 1 that ports 12a, 12b and 12c are supposed to be a single set, not "at least two of said plurality of sets" as in claim 7.

CLAIM 29

Claim 29 is reprinted as follows for convenience:

The method of claim 16, **wherein each second node in said plurality of sets of second nodes is configured with at least two communications ports.**

Again, Appellant strongly disagrees with the interpretation of claim language applied by the Examiner. The Examiner has indicated that Baty's port 12a is a second node as in Appellant's claim 11, and that the connections from port 12a on trace 46a and bus 26 are communications ports on Baty's port 12a. Baty's ports thus each have two ports. Appellant believes that the Examiner has applied such broad interpretations of terms in both Appellant's claims and Baty's disclosure that the meanings given in both documents become meaningless.

CLAIM 30

Claim 30 is reprinted as follows for convenience:

The method of claim 16, **further comprising partitioning connections among second nodes in said plurality of sets of second nodes into a plurality of incomplete fabrics.**

The Examiner takes the position that Baty's ports 12a and 12b are connected by interface section 40 and processing section 42, and that this comprises an incomplete fabric. Appellant respectfully disagrees that Baty's interface section 40 and processing section 42 comprise a fabric of any sort that connects ports 12a and 12b. Baty does not disclose or suggest that communications pass between ports 12a and 12b via

interface section 40 and processing section 42.

CLAIM 31

Solely for the purposes of this appeal, claim 31 stands or falls with claim 16.

CLAIM 32

Claim 32 is reprinted as follows for convenience:

A method for converting a mathematical design to a physical communications network, comprising:

providing a mathematical representation of a plurality of connected first nodes in the form of a balanced incomplete block design defined as 2-(v, k, 1) = b, wherein v first nodes, arranged in b groups of k first nodes, are interconnected such that a pair of first nodes appears in only one group of the b groups;

converting the mathematical representation to a physical design in which a plurality of first forwarding nodes interconnect the plurality of first nodes; and

assigning a plurality of sets of second nodes to one of the first nodes; such that each of the second nodes is interconnected to every other node.

As discussed above with respect to claim 1, the computing system architecture of claim 10 is allowable at least because Baty does not disclose or suggest a plurality of sets of second nodes being interconnected with a plurality of first nodes. Baty's ports (e.g., 12a) are not nodes as defined either in Applicant's specification or by Baty.

Baty also does not disclose or suggest providing a mathematical representation of the plurality of first nodes in

the BIBD design and converting the mathematical representation to a physical design.

Appellant therefore believes that claim 32 is allowable over the cited references and respectfully requests reversal of the rejection.

CLAIM 33

Solely for the purposes of this appeal, claim 33 stands or falls with claim 32.

CLAIM 34

Claim 34 is reprinted as follows for convenience:

The method of claim 32, **wherein each of said plurality of connected first nodes includes at least one switch.**

The Examiner takes the position that Baty's processing section 42 comprises a switch on a node. Appellant respectfully disagrees. Baty teaches that the processing sections on the nodes 12-24 are "functional units of a digital data processing system" (col. 4, lines 48-50) including three central processing units, a network interface, two peripheral controllers and a shared random access memory unit (col. 4, lines 50-54). Baty clearly does not disclose that "each first node includes at least one first switch." The Examiner has cited Baty, col. 5, lines 12-31 as disclosing the interconnection of second nodes by a switch on a node. However, this section of Baty interface circuitry on each node that determines which port to send communications from. This clearly does not disclose the interconnection of second nodes by a switch on a node.

CLAIM 35

Claim 35 is reprinted as follows for convenience:

The method of claim 34, **further comprising configuring interconnections of each second node of said plurality of sets of second nodes to other second nodes via said at least one switch.**

Again, Baty does not disclose that "each first node includes at least one first switch." Baty teaches that the processing sections on the nodes 12-24 are "functional units of a digital data processing system" (col. 4, lines 48-50) including three central processing units, a network interface, two peripheral controllers and a shared random access memory unit (col. 4, lines 50-54). Baty also does not teach that each second node is interconnected to other second nodes by a switch on a first node. Even if Baty's ports (e.g., 12a) anticipate the claimed second nodes, Baty clearly does not teach that each port is interconnected to other ports by a switch on the first node, particularly with the network connections addressed in Appellant's claims. For example, Baty's random access memory unit is clearly not a switch that performs network interconnections of the three ports on the random access memory unit node. The Examiner has cited Baty, col. 5, lines 12-31 as disclosing the interconnection of second nodes by a switch on a node. However, this section of Baty interface circuitry on each node that determines which port to send communications from. This clearly does not disclose the interconnection of second nodes by a switch on a node.

CLAIM 36

Claim 36 is reprinted as follows for convenience:

The method of claim 34, **wherein said at least one switch interconnects one of said plurality of sets of second nodes to another of said plurality of sets of second nodes.**

Again, Baty does not disclose that "each first node includes at least one first switch." Baty teaches that the processing sections on the nodes 12-24 are "functional units of a digital data processing system" (col. 4, lines 48-50) including three central processing units, a network interface, two peripheral controllers and a shared random access memory unit (col. 4, lines 50-54). Baty also does not teach that each second node is interconnected to other second nodes by a switch on a first node. Even if Baty's ports (e.g., 12a) anticipate the claimed second nodes, Baty clearly does not teach that each port is interconnected to other ports by a switch on the first node, particularly with the network connections addressed in Appellant's claims. For example, Baty's random access memory unit is clearly not a switch that performs network interconnections of the three ports on the random access memory unit node. Furthermore, if the three ports on each of Baty's nodes comprise a set as indicated by the Examiner with respect to claim 1, then the processing section (e.g., 42) on one node (e.g., 12) would not act as a switch to connect a port (e.g., 12a) on that node (e.g., 12) with a port (e.g., 14a) on another node (e.g., 14). The Examiner has cited Baty, col. 5, lines 12-31 as disclosing the interconnection of second nodes by a switch on a node. However, this section of Baty interface circuitry on each node that determines which port to send communications from. This clearly does not disclose the interconnection of second nodes

by a switch on a node.

CLAIM 37

Claim 37 is reprinted as follows for convenience:

The method of claim 34, **wherein at least one of said at least one second switches is shared by at least two of said plurality of sets of second nodes.**

Again, Baty does not disclose that "each first node includes at least one first switch." Baty teaches that the processing sections on the nodes 12-24 are "functional units of a digital data processing system" (col. 4, lines 48-50) including three central processing units, a network interface, two peripheral controllers and a shared random access memory unit (col. 4, lines 50-54). Furthermore, if the three ports on each of Baty's nodes comprise a set as indicated by the Examiner with respect to claim 1, then the processing section (e.g., 42) on one node (e.g., 12) would not be shared with at least two of the plurality of sets of second nodes. For example, set 12a, 12b and 12c does not share processing section 42 with set 14a, 14b and 14c. The Examiner has stated with respect to claim 7 that "the switch in node 12 is shared with 12a, 12b and 12c". However, the Examiner indicated with respect to claim 1 that ports 12a, 12b and 12c are supposed to be a single set, not "at least two of said plurality of sets" as in claim 7.

CLAIM 41

Claim 41 is reprinted as follows for convenience:

The method of claim 32, **wherein each second node in said**

plurality of sets of second nodes is configured with at least two communications ports.

Again, Appellant strongly disagrees with the interpretation of claim language applied by the Examiner. The Examiner has indicated that Baty's port 12a is a second node as in Appellant's claim 11, and that the connections from port 12a on trace 46a and bus 26 are communications ports on Baty's port 12a. Baty's ports thus each have two ports. Appellant believes that the Examiner has applied such broad interpretations of terms in both Appellant's claims and Baty's disclosure that the meanings given in both documents become meaningless.

CLAIM 42

Claim 42 is reprinted as follows for convenience:

The method of claim 32, **further comprising partitioning connections among second nodes in said plurality of sets of second nodes into a plurality of incomplete fabrics.**

The Examiner takes the position that Baty's ports 12a and 12b are connected by interface section 40 and processing section 42, and that this comprises an incomplete fabric. Appellant respectfully disagrees that Baty's interface section 40 and processing section 42 comprise a fabric of any sort that connects ports 12a and 12b. Baty does not disclose or suggest that communications pass between ports 12a and 12b via interface section 40 and processing section 42.

CLAIM 43

Solely for the purposes of this appeal, claim 43 stands or falls with claim 32.

II. Rejection of claims 8-10, 15, 22-28 and 38-40 stand rejected under 35 U.S.C. 103(a)

CLAIMS 8-10 and 15

Solely for the purposes of this appeal, claims 8-10 and 15 stand or fall with claim 1.

CLAIMS 22-28

Solely for the purposes of this appeal, claims 22-28 stand or fall with claim 16.

CLAIMS 38-40

Solely for the purposes of this appeal, claims 38-40 stand or fall with claim 32.

III. Rejection of claim 44 under 35 U.S.C. 103(a)

CLAIM 44

Solely for the purposes of this appeal, claim 44 stands or falls with claim 32.

In view of the above, all of the claims are believed to be in condition for allowance, and the Appellant respectfully requests reversal of the rejection.

Respectfully submitted,
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Claims Appendix

1. (Original) A multi-fabric interconnection system, comprising:

a plurality of first nodes interconnected as a balanced incomplete block design of the form 2-(v, k, 1) = b, wherein v first nodes, arranged in b groups of k first nodes, are interconnected such that each pair of first nodes appears in only one group of the b groups, and

a plurality of first forwarding nodes configured to interconnect the plurality of first nodes;

a plurality of sets of second nodes, wherein each second node is connected to one of the first nodes, and wherein each of the second nodes is interconnected to every other second node.

2. (Original) The interconnection system of claim 1, wherein each second node is interconnected to other second nodes via at least one first node.

3. (Original) The interconnection system of claim 1, wherein each first node includes at least one first switch.

4. (Original) The interconnection system of claim 3, wherein each second node in said plurality of sets of second nodes is interconnected to other second nodes via said at least one first switch.

5. (Original) The interconnection system of claim 4, wherein each of said plurality of sets of second nodes is interconnected to another of said plurality of sets of second nodes via said at least one first switch.

6. (Original) The interconnection system of claim 4, wherein said at least one first switch interconnects one of said plurality of sets of second nodes to another of said plurality of sets of second nodes.

7. (Original) The interconnection system of claim 4, wherein said at least one first switch is shared with at least two of said plurality of sets of second nodes.

8. (Original) The interconnection system of claim 1, wherein each of said plurality of sets of second nodes is further divided into a plurality of sub-sets of second nodes.

9. (Original) The interconnection system of claim 8, wherein said plurality of sub-sets of second nodes in at least one of said plurality of sets of second nodes are interconnected to each other via a second switch.

10. (Original) The interconnection system of claim 8, wherein said plurality of sub-sets of second nodes are interconnected to each other via at least one of said at least one first switches within one of said plurality of first nodes.

11. (Original) The interconnection system of claim 1, wherein each second node in said plurality of sets of second nodes is configured with at least two communications ports.

12. (Original) The interconnection system of claim 1, wherein connections between second nodes in said plurality of sets of second nodes are partitioned into a plurality of incomplete fabrics.

13. (Original) The interconnection system of claim 1, wherein at least one of said plurality of first forwarding nodes are chosen from a group consisting of routers, switches, crossbars, optical rings, backplanes, buses, interconnections, and links.

14. (Original) The interconnection system of claim 1, wherein each second node in said plurality of sets of second nodes is interconnected to every other second node via at least one of said plurality of first nodes.

15. (Original) The interconnection system of claim 8, wherein said plurality of sub-sets of second nodes are interconnected to each other via one of said plurality of first forwarding nodes.

16. (Original) A method for configuring a communications network, comprising:

configuring interconnections of a plurality of first nodes as a balanced incomplete block design of the form 2-(v, k, 1) = b, wherein v first nodes, arranged in b groups of k first nodes, are interconnected such that a pair of first nodes appears in only one group of the b groups; and

configuring interconnections of a plurality of sets of second nodes to the plurality of first nodes, wherein each second node is interconnected to every other second node.

17. (Original) The method of claim 16, further comprising configuring interconnections of each second node in said plurality of sets of second nodes to every other second node via at least one of said plurality of first nodes.

18. (Original) The method of claim 16, wherein each of said plurality of first nodes includes at least one switch.

19. (Original) The method of claim 18, further comprising configuring interconnections of each second node in said plurality of sets of second nodes to every other second node via said at least one switch.

20. (Original) The method of claim 18, wherein said at least one switch interconnects one set of second nodes in said plurality of sets of second nodes to another set of second nodes in said plurality of sets of second nodes.

21. (Original) The method of claim 18, wherein at least one of said at least one switches is shared by at least two sets of second nodes in said plurality of sets of second nodes.

22. (Original) The method of claim 16, further comprising dividing said plurality of sets of second nodes into a plurality of sub-sets of second nodes.

23. (Original) The method of claim 22, further comprising configuring a plurality of first forwarding nodes to interconnect said plurality of first nodes.

24. (Original) The method of claim 23, wherein at least one of said plurality of first forwarding nodes is chosen from a group consisting of routers, switches, crossbars, optical rings, backplanes, buses, interconnections, and links.

25. (Original) The method of claim 23, further comprising configuring interconnections of each of said plurality of sub-sets of second nodes to other sub-sets of second nodes via one of said plurality of first forwarding nodes.

26. (Original) The method of claim 23, further comprising configuring a plurality of second forwarding nodes to interconnect said plurality of sets of second nodes.

27. (Original) The method of claim 26, wherein at least one of said plurality of second forwarding nodes is chosen from a group consisting of routers, switches, crossbars, optical rings, backplanes, buses, interconnections, and links.

28. (Original) The method of claim 22, further comprising configuring interconnections of each of said plurality of sub-sets of second nodes to other sub-sets of second nodes via a switch within one of said plurality of first nodes.

29. (Original) The method of claim 16, wherein each second node in said plurality of sets of second nodes is configured with at least two communications ports.

30. (Original) The method of claim 16, further comprising partitioning connections among second nodes in said plurality of sets of second nodes into a plurality of incomplete fabrics.

31. (Original) The method of claim 16, wherein each second node in said plurality of sets of second nodes is connected to one of said plurality of first nodes.

32. (Original) A method for converting a mathematical design to a physical communications network, comprising:

providing a mathematical representation of a plurality of connected first nodes in the form of a balanced incomplete block design defined as 2-(v, k, 1) = b, wherein v first nodes, arranged in b groups of k first nodes, are interconnected such that a pair of first nodes appears in only

one group of the *b* groups;

converting the mathematical representation to a physical design in which a plurality of first forwarding nodes interconnect the plurality of first nodes; and

assigning a plurality of sets of second nodes to one of the first nodes; such that each of the second nodes is interconnected to every other node.

33. (Original) The method of claim 32, further comprising interconnecting each second node of said plurality of sets of second nodes to other second nodes via at least one of said plurality of connected first nodes.

34. (Original) The method of claim 32, wherein each of said plurality of connected first nodes includes at least one switch.

35. (Original) The method of claim 34, further comprising configuring interconnections of each second node of said plurality of sets of second nodes to other second nodes via said at least one switch.

36. (Original) The method of claim 34, wherein said at least one switch interconnects one of said plurality of sets of second nodes to another of said plurality of sets of second nodes.

37. (Original) The method of claim 34, wherein at least one of said at least one second switches is shared by at least two of said plurality of sets of second nodes.

38. (Original) The method of claim 32, further comprising dividing said plurality of sets of second nodes into a plurality of sub-sets of second nodes.

39. (Original) The method of claim 38 further comprising configuring interconnections of each of said plurality of sub-sets of second nodes to other sub-sets of second nodes via a switch.

40. (Original) The method of claim 39, wherein said switch is within one of said plurality of connected first nodes.

41. (Original) The method of claim 32, wherein each second node in said plurality of sets of second nodes is configured with at least two communications ports.

42. (Original) The method of claim 32, further comprising partitioning connections among second nodes in said plurality of sets of second nodes into a plurality of incomplete fabrics.

43. (Original) The method of claim 32, wherein at least one of said plurality of first forwarding nodes is chosen from a group consisting of routers, switches, crossbars, optical rings, backplanes, buses, interconnections, and links.

44. (Original) The method of claim 32, wherein said method is executed recursively.

Evidence Appendix

None.

Related Proceedings Appendix

None.